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Serial No: 10/751,198

Amendments to the Claims

1. (Currently Amended) A method for packaging a multi-chip module, comprising the steps of:

connecting wafer bumps in a peripheral region of a first chip ~~having thereon wafer bumps~~ to lower parts of inner leads of first and second TAB tapes, each of the first and second TAB tapes having an inner lead and an outer lead~~, thereby electrical signals being communicated therebetween~~;

connecting wafer bumps in a peripheral region of a second chip ~~having thereon wafer bumps~~ to upper parts of the inner leads of the first and second TAB tapes connected to the first chip, thereby electrical signals being communicated therebetween;

~~executing an encapsulation step, wherein an underfill material is filled in connecting portions between the TAB tapes and the chips; and~~

~~mounting the outer lead of one of~~ the first TAB tape[[s]] on a patterned circuit;

connecting a third chip having thereon wafer bumps to an upper part of the second chip;

connecting an outer lead of the second TAB tape to at least one of the wafer bumps in a peripheral region of the third chip;

connecting an inner lead of a third TAB tape having the inner lead and an outer lead to at least one other wafer bump in the peripheral region of the third chip;

connecting wafer bumps in a peripheral region of a fourth chip to the outer lead of the second TAB tape and the inner lead of the third TAB tape; and

executing at least one encapsulation step, wherein an underfill material is filled in connecting portions between the first, second and third TAB tapes and the first, second, third and fourth chips.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The method of claim 1, further comprising the steps of coating a first conductive adhesive on the upper part of the second chip and mounting a radiator on the first conductive adhesive~~after a conductive adhesive is coated on an upper part of the second chip~~.

5. (Original) The method of claim 1, wherein the chips and the TAB tapes are connected to each other by using gang bonding or single point bonding method.

6. (Original) The method of claim 5, wherein the chips and the TAB tapes are connected to each other by bonding the inner leads of the TAB tapes to the wafer bumps of the chips.

7. (Cancelled)

8. (Currently Amended) The method of claim [[2]]4, further comprising the steps of coating a second conductive adhesive on the upper part of the fourth chip and mounting a radiator ~~after a conductive adhesive is coated~~ on ~~an upper part of~~ the second conductive adhesive~~chip~~.

9. (Currently Amended) The method of claim [[2]]8, wherein the chips and the TAB tapes are connected to each other by using gang bonding or single point bonding method.

10. (Original) The method of claim 9, wherein the chips and the TAB tapes are connected to each other by bonding the inner leads of the TAB tapes to the wafer bumps of the chips.

11. (Currently Amended) The method of claim [[2]]1, further comprising the step of ~~accumulating a plurality of chips having thereon wafer bumps and a plurality of~~ connecting the

outer lead of the third TAB tape[[s]] ~~having an inner lead and an outer lead on the fourth chip~~ patterned circuit.